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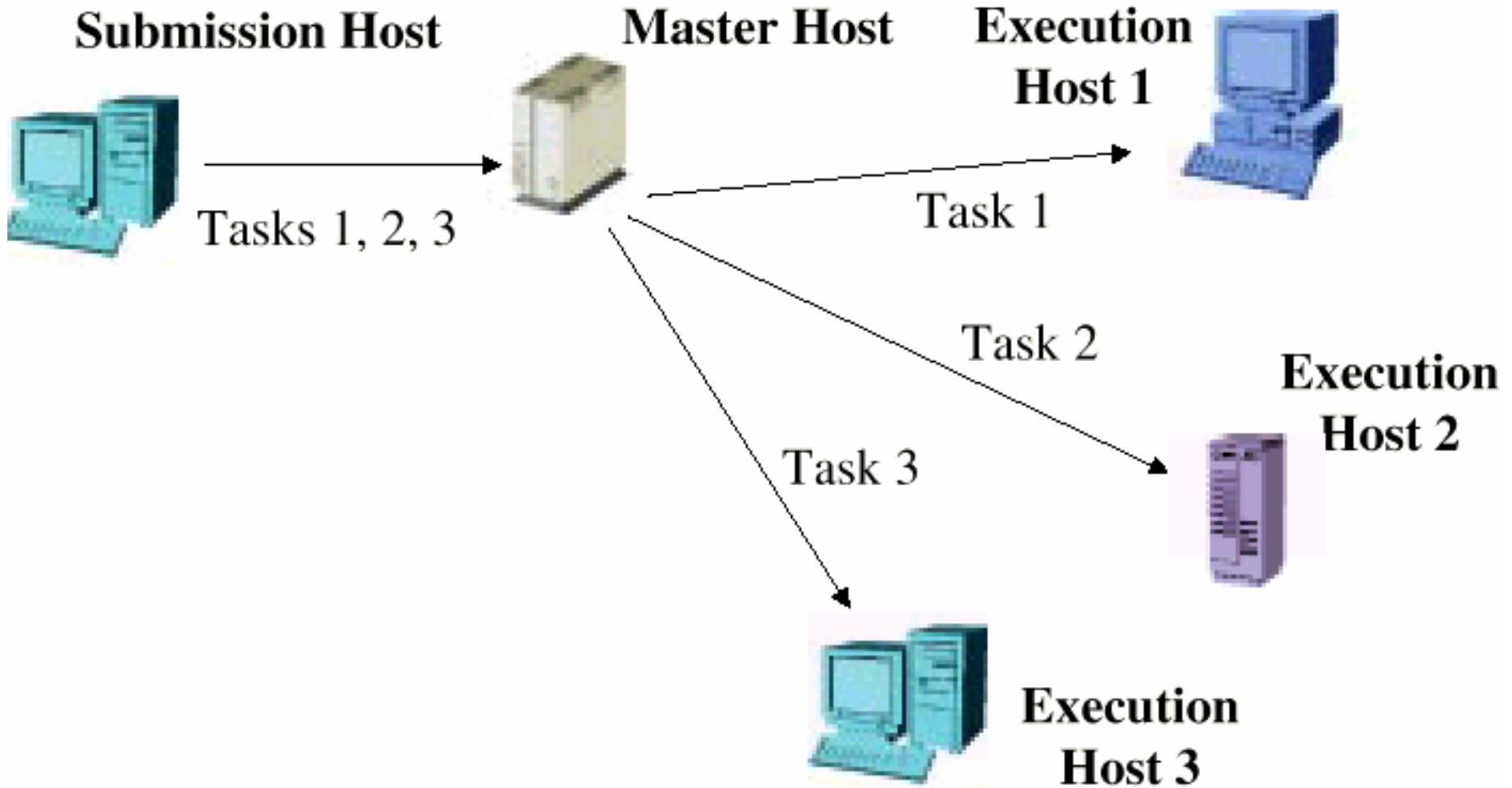
² George Mason University

**Job Management System
Extension
to Support SLAAC-1V
Reconfigurable Hardware**

Problem:

- Reconfigurable resources expensive and unutilized
- Many of these resources available over the network
- It is desirable to leverage networked reconfigurable resources to help other users within the same organization

Approach of Job Management System



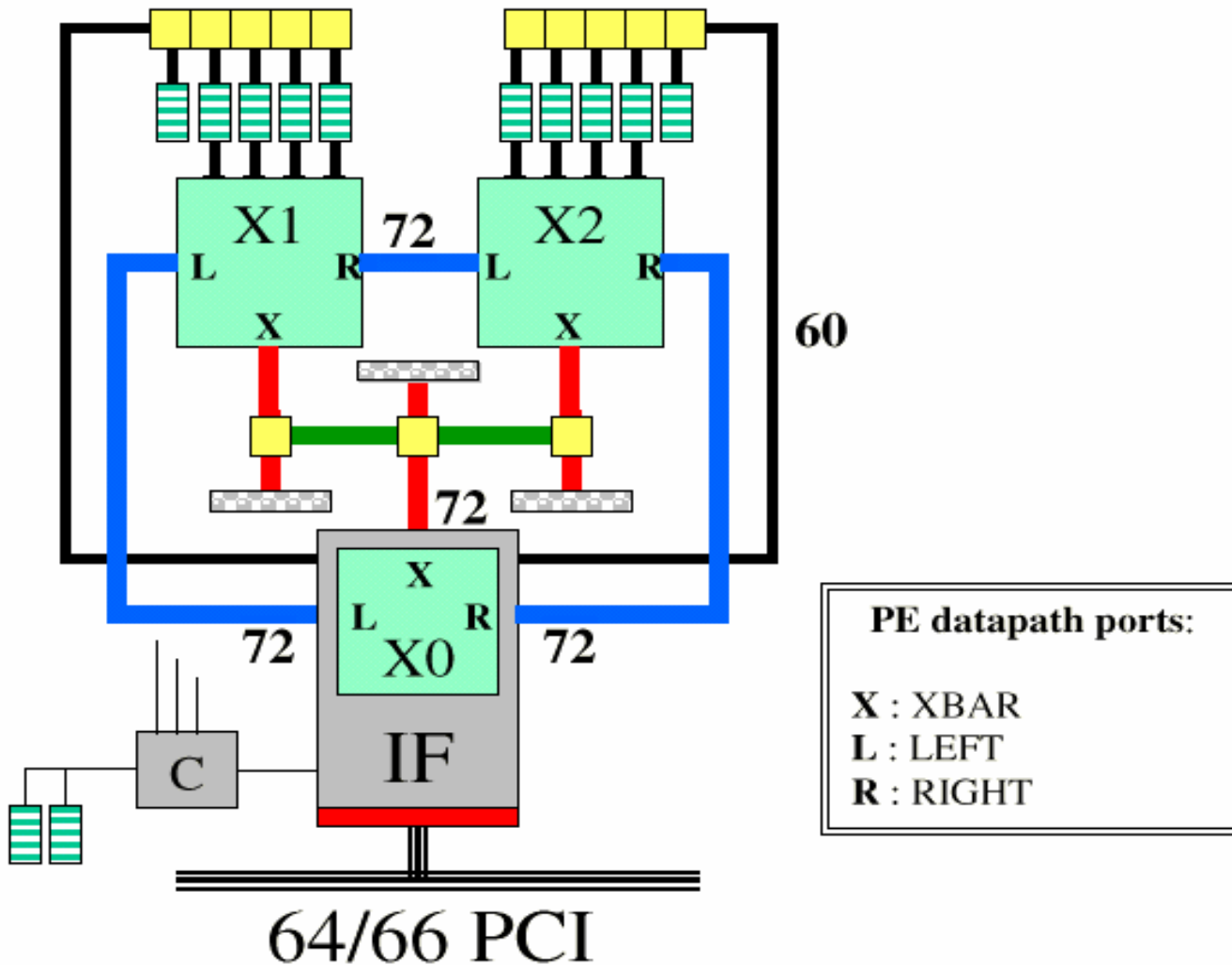
LSF

- The LSF Suite (Load Sharing Facility) is an industry-standard set of integrated products that manage distributed computing resources and workloads.
- LSF is a layer of software services on top of UNIX and Windows NT operating systems.
- LSF creates a single system image on a network of heterogeneous computers so that the whole network of computing resources can be utilized effectively and managed easily.

SLAAC1-V

- Full-sized 64-bit PCI card.
- Three Xilinx XCV1000-6 compute FPGAs
- The memories are 36x256K ZBT SRAMs.

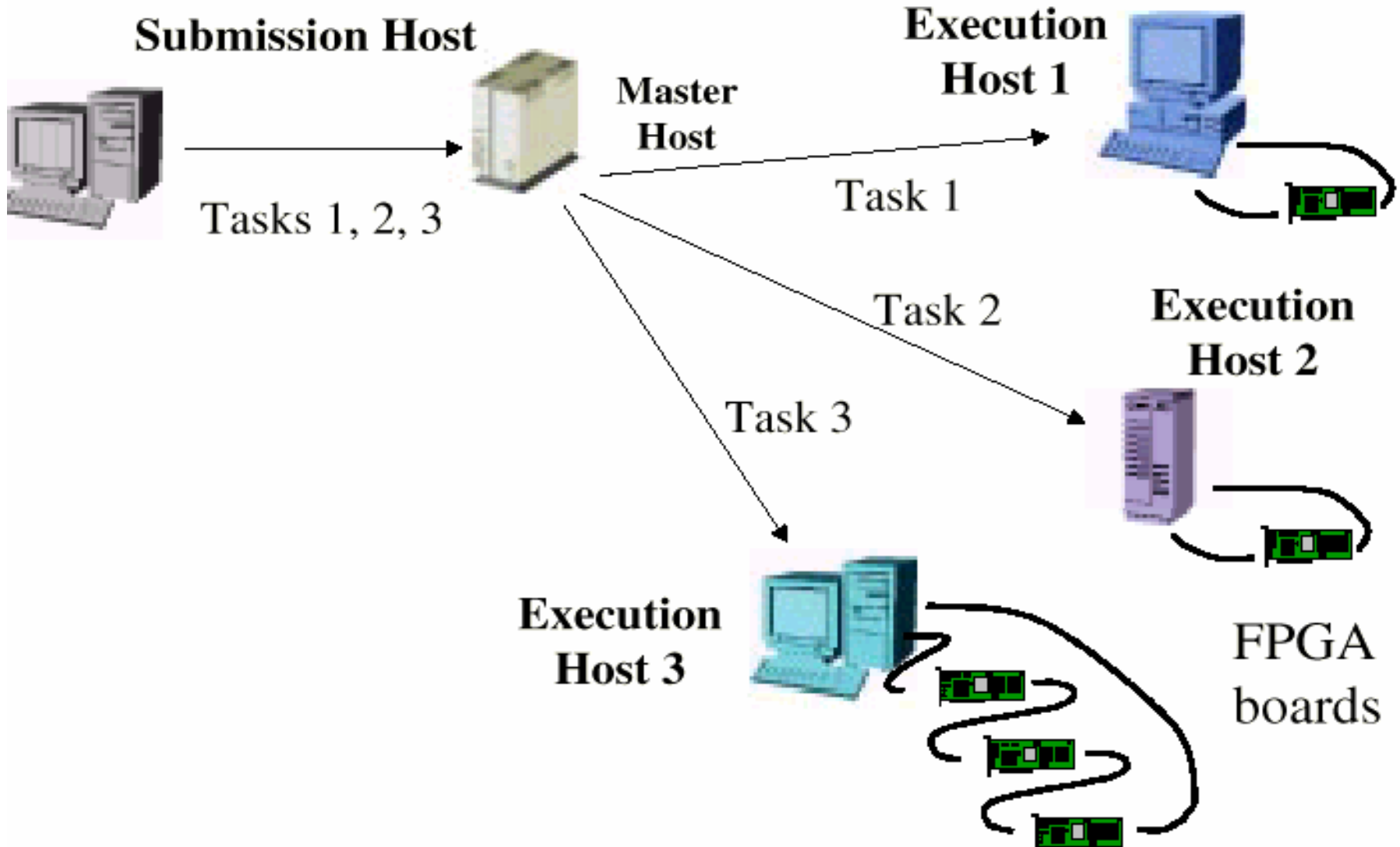
SLAAC1-V Top Level Block Diagram



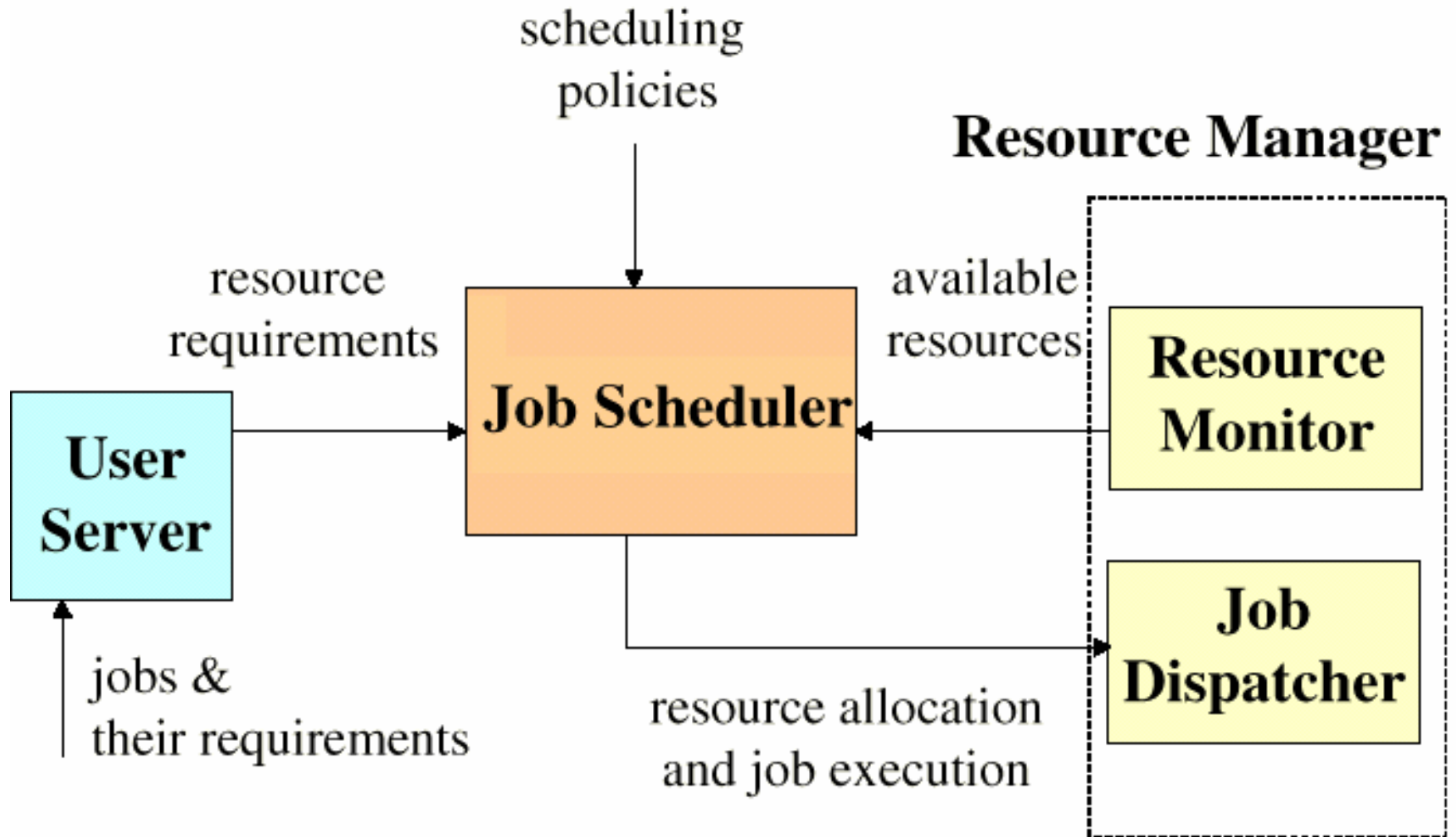
Approach

- **Extend LSF to recognize and utilize SLAAC1-V reconfigurable resources**
 - add new dynamic resources
 - configure scheduling to be based on these new resources

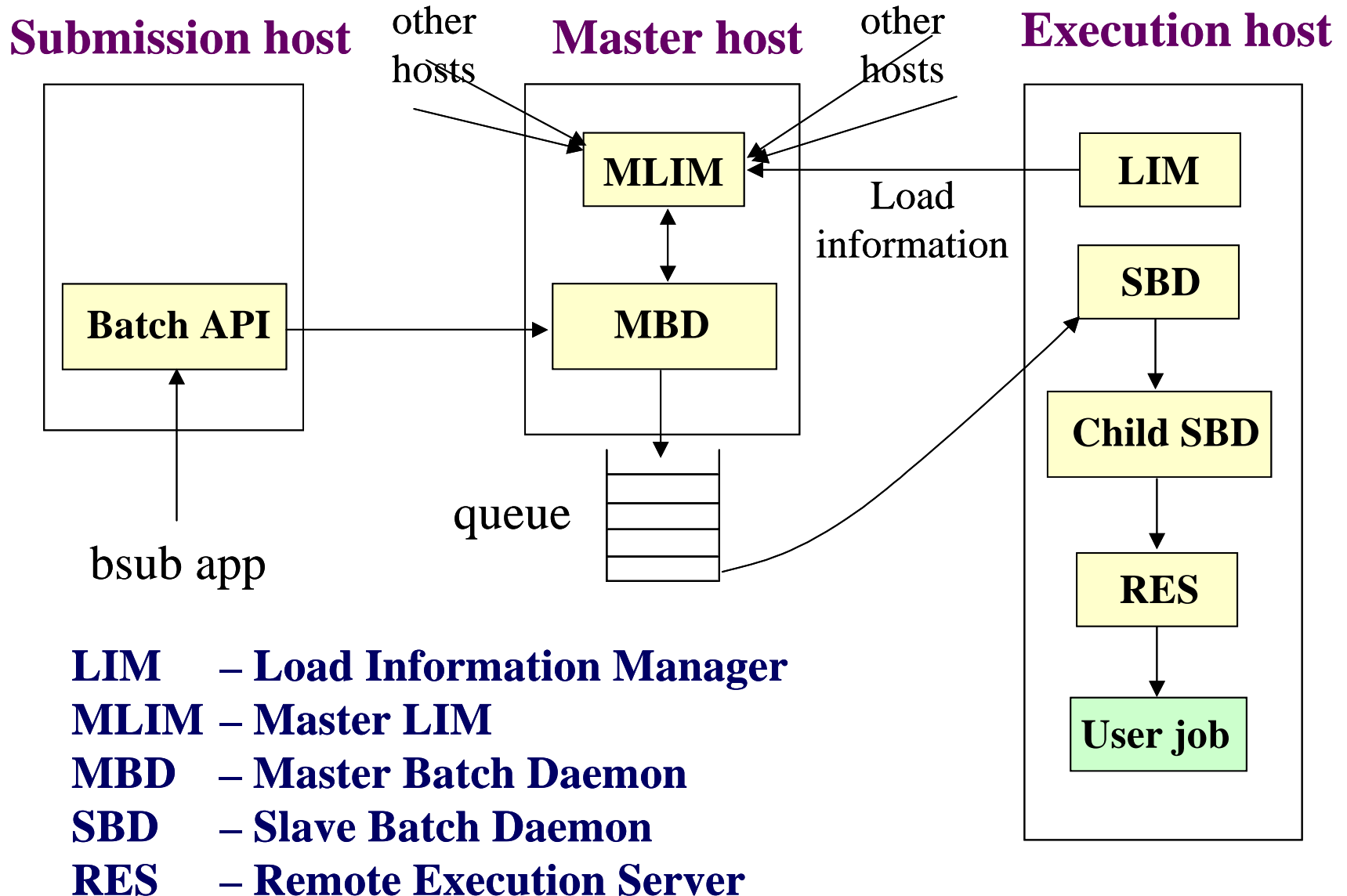
Networked Reconfigurable Resource Management System



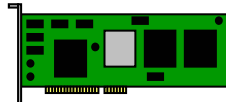
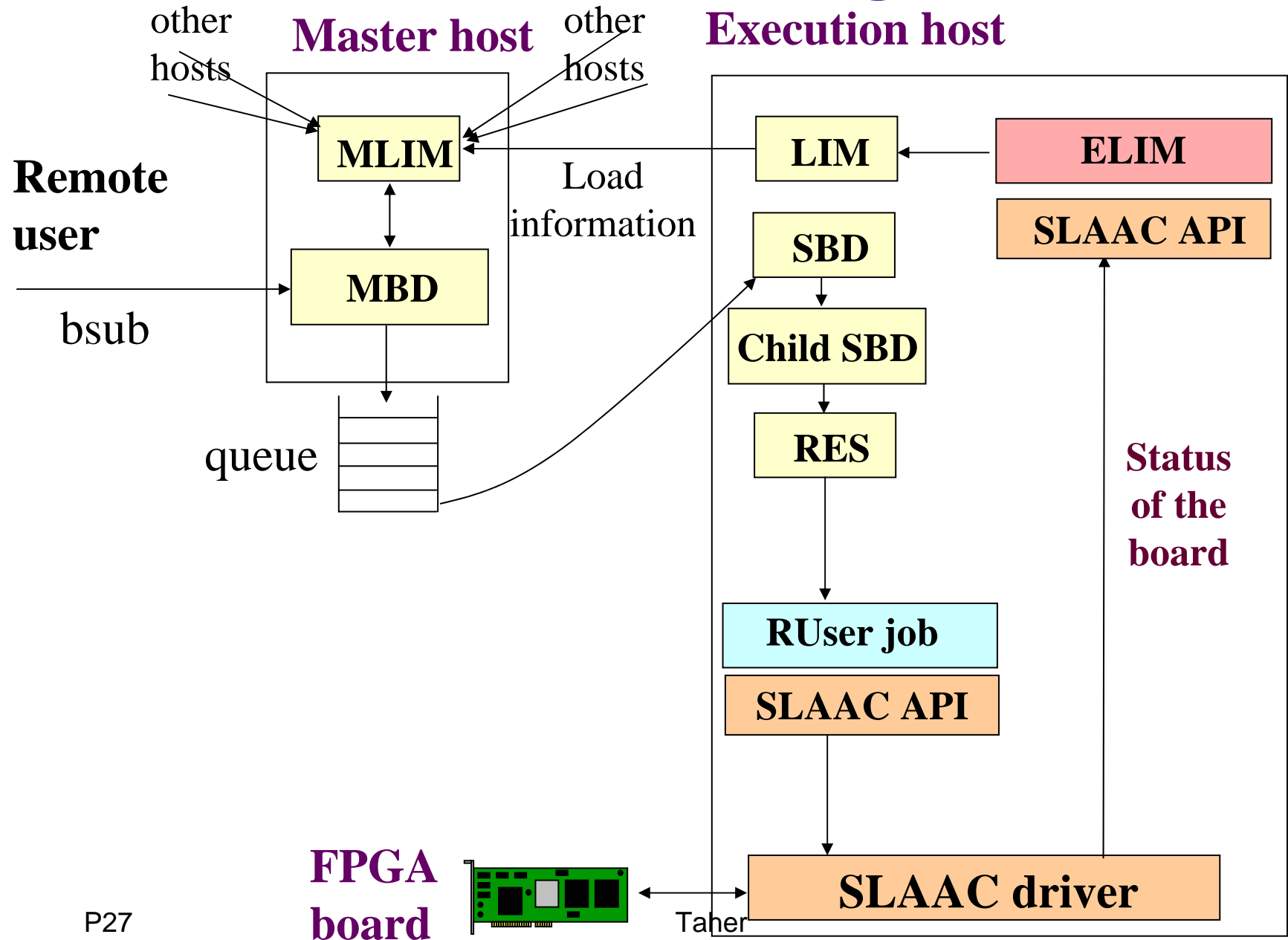
LSF Structure



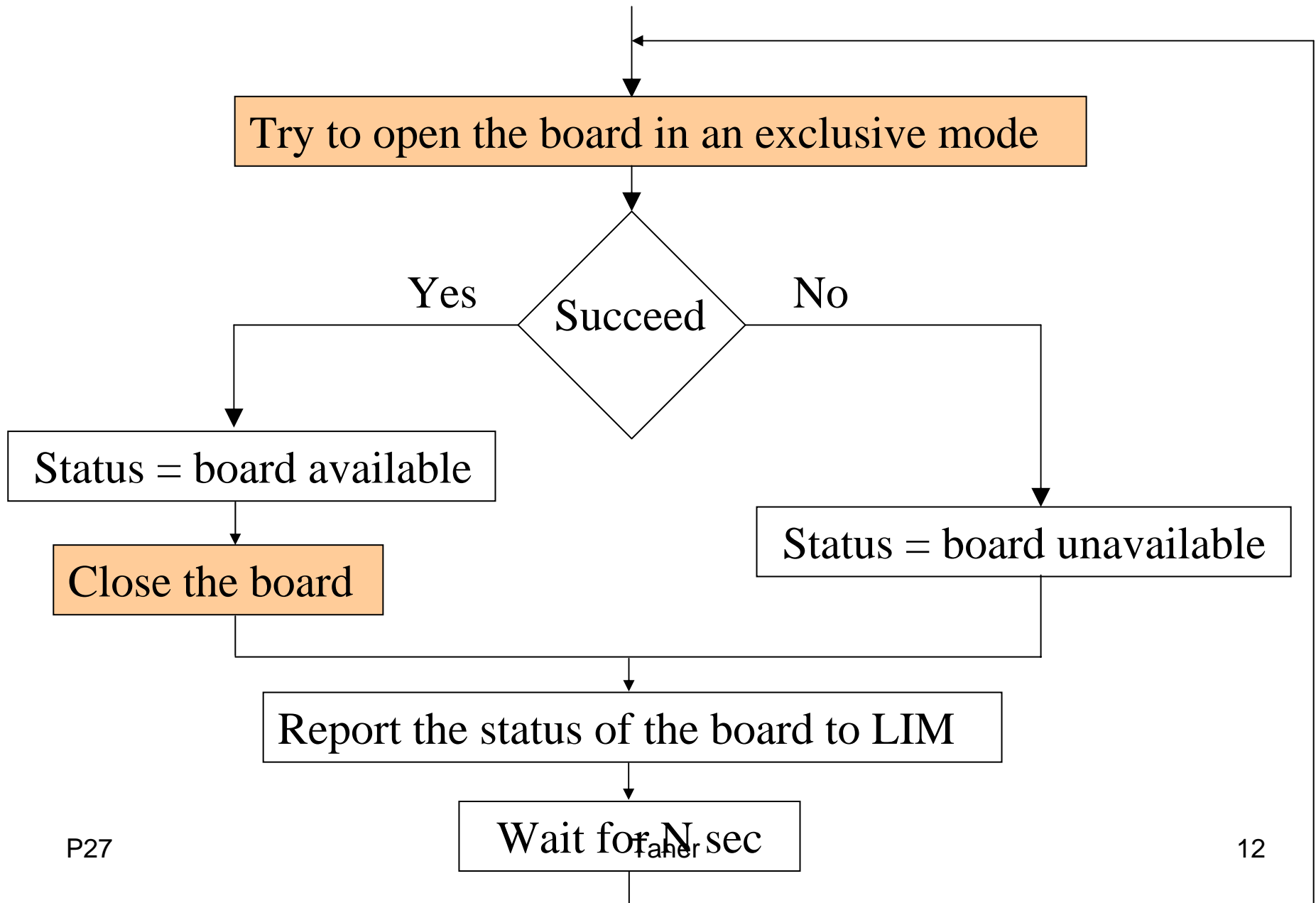
General Architecture of LSF



Extension of LSF to reconfigurable hardware

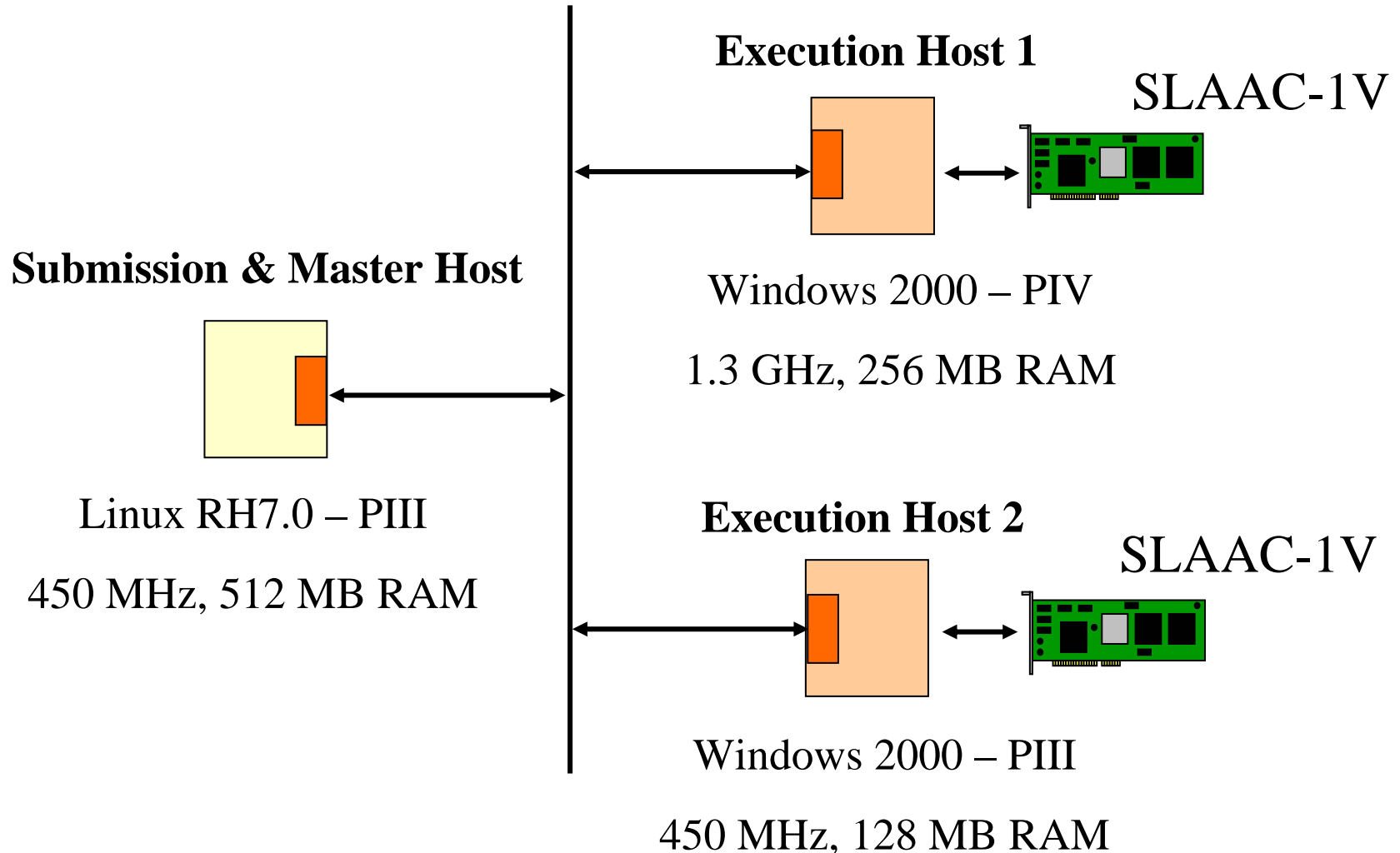


Operation of ELIM



Experimental verification

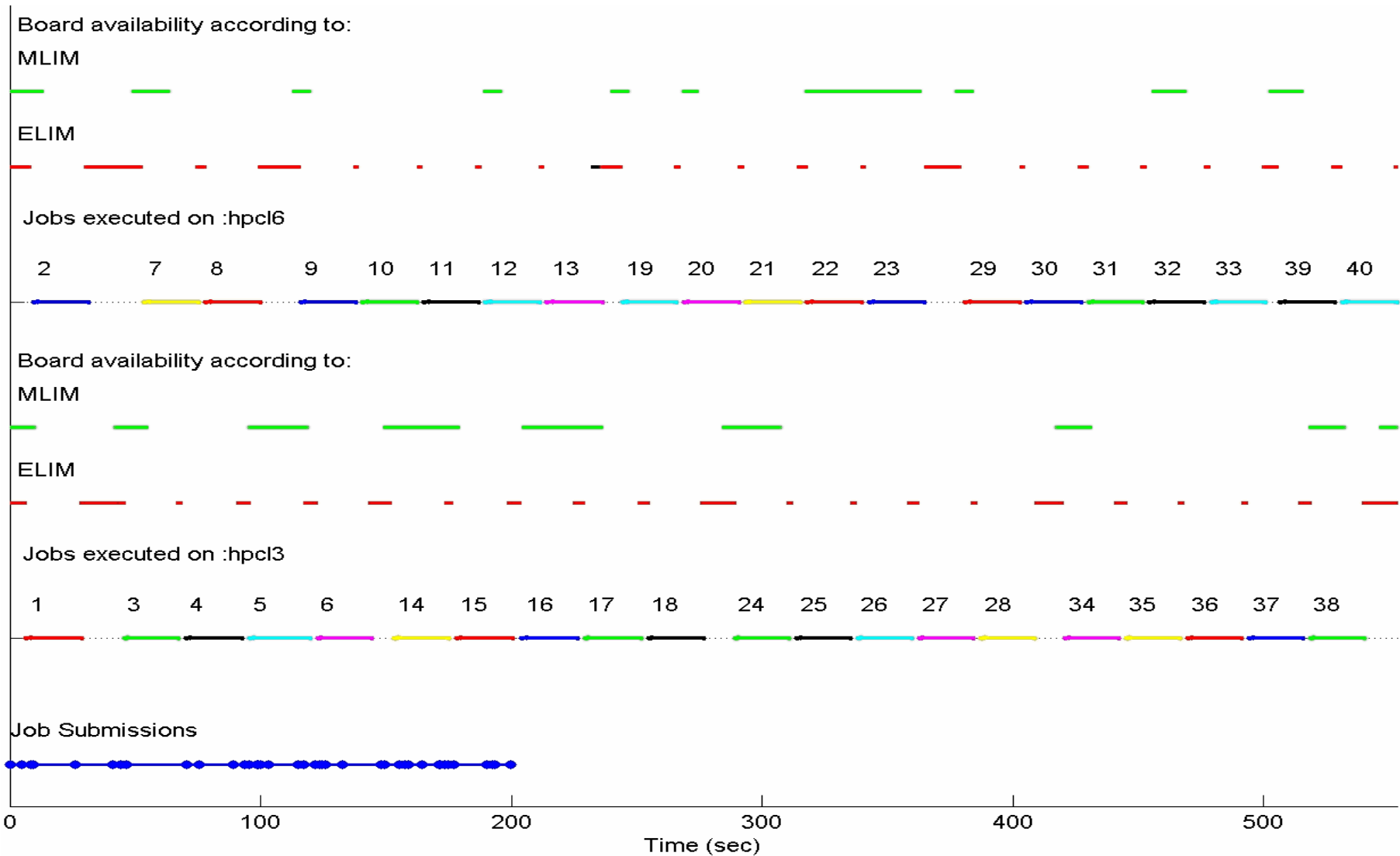
Testbed used in the experiments



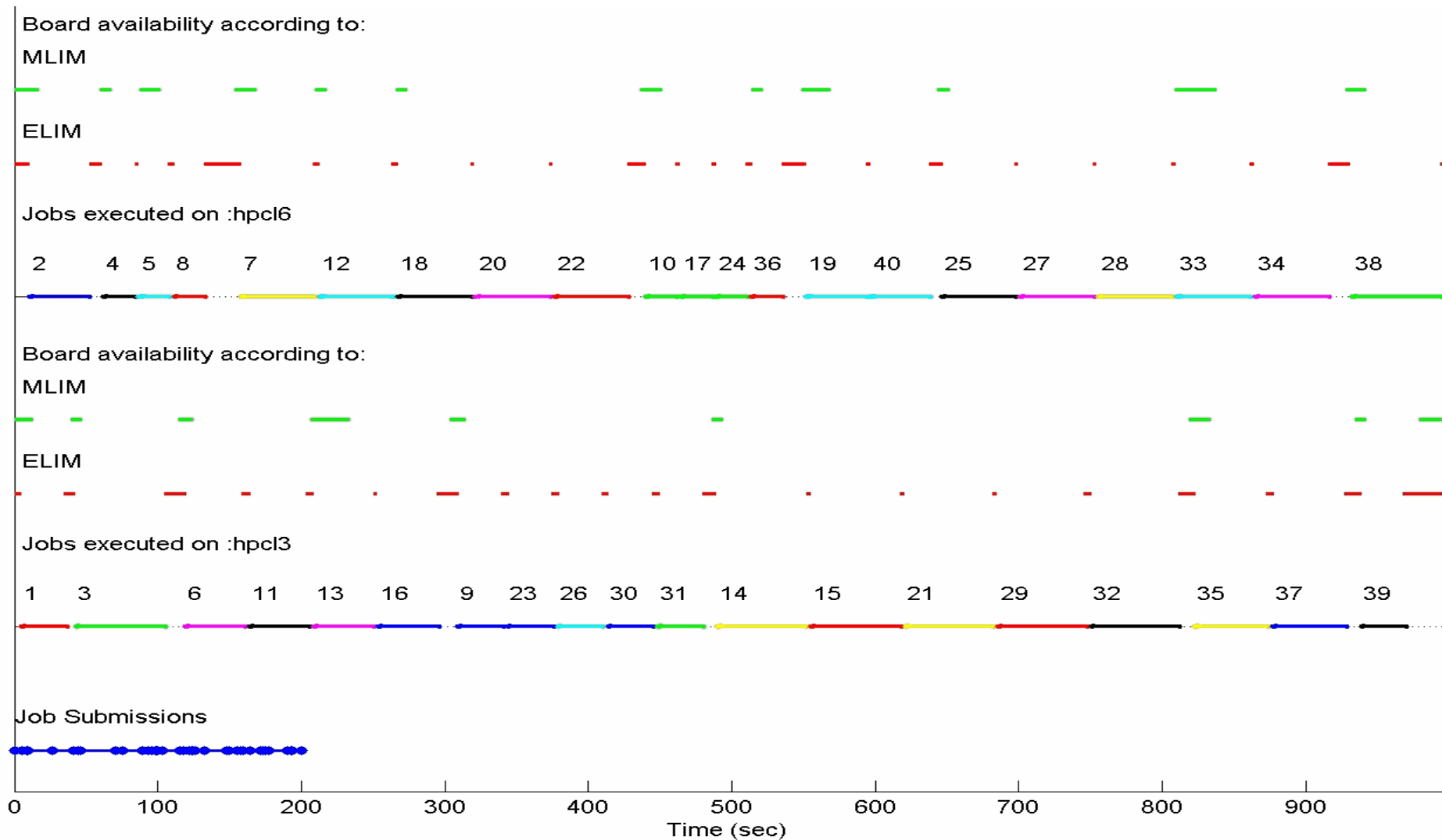
Parameters of Performed Experiments

Exp. No.	No. of execution hosts	Number and execution times of jobs	Delay between job submissions
1	2	40 x 20 s	5 s
2	2	8 x 20 s, 8 x 30 s, 8 x 40 s, 8 x 50 s, 8 x 60 s	5 s
3	2	40 x 120 s	5 s
4	2	40 x 300 s	5 s
5	2	3 x 20 s 3 x 40 s 3 x 60 s 3 x 80 s 3 x 100 s 3 x 120 s 3 x 140 s 3 x 160 s 3 x 180 s 3 x 200 s 3 x 220 s 3 x 240 s 3 x 260 s 3 x 280 s 3 x 300 s	5 s

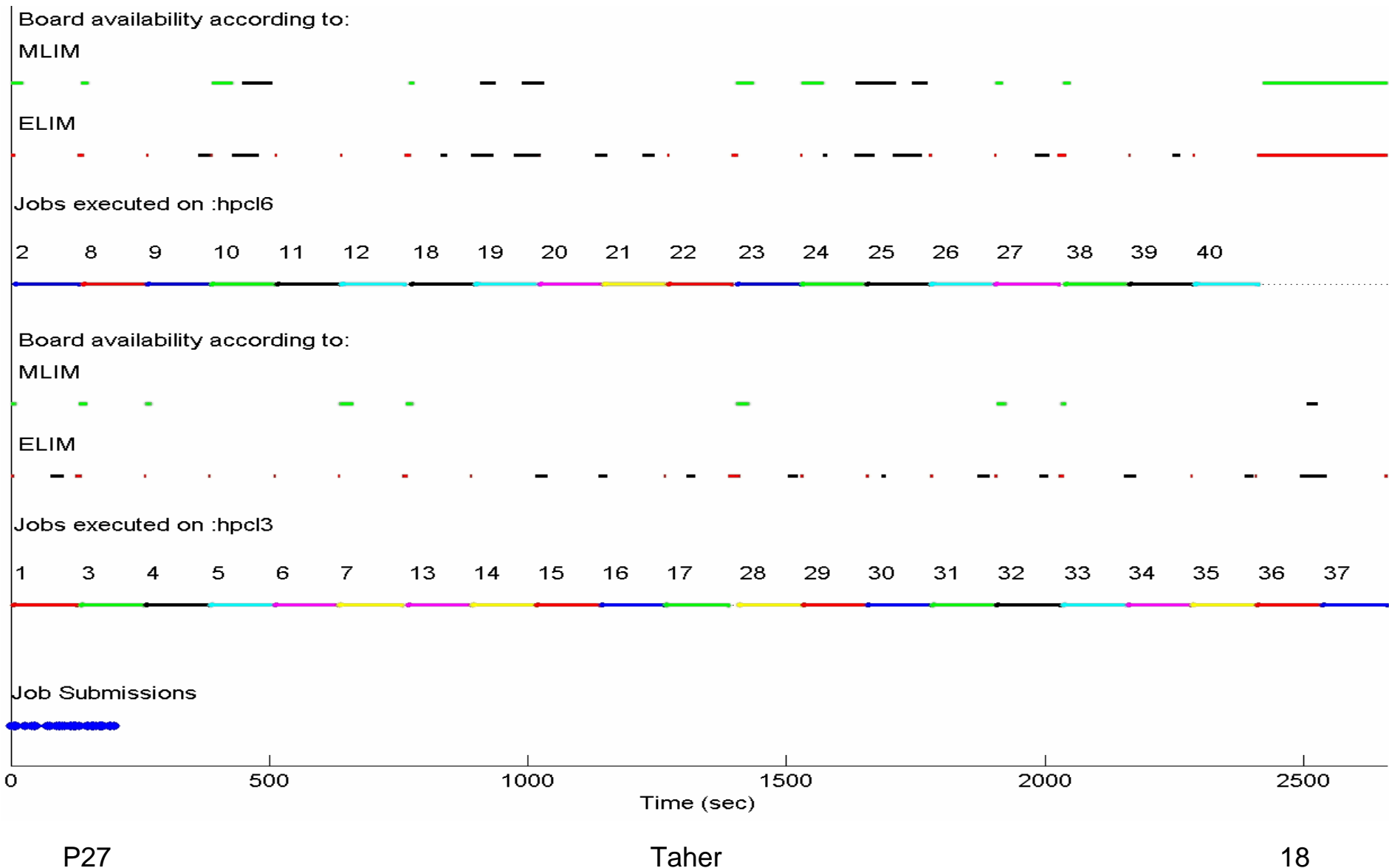
Utilization of machines in Experiment 1, Iteration 1



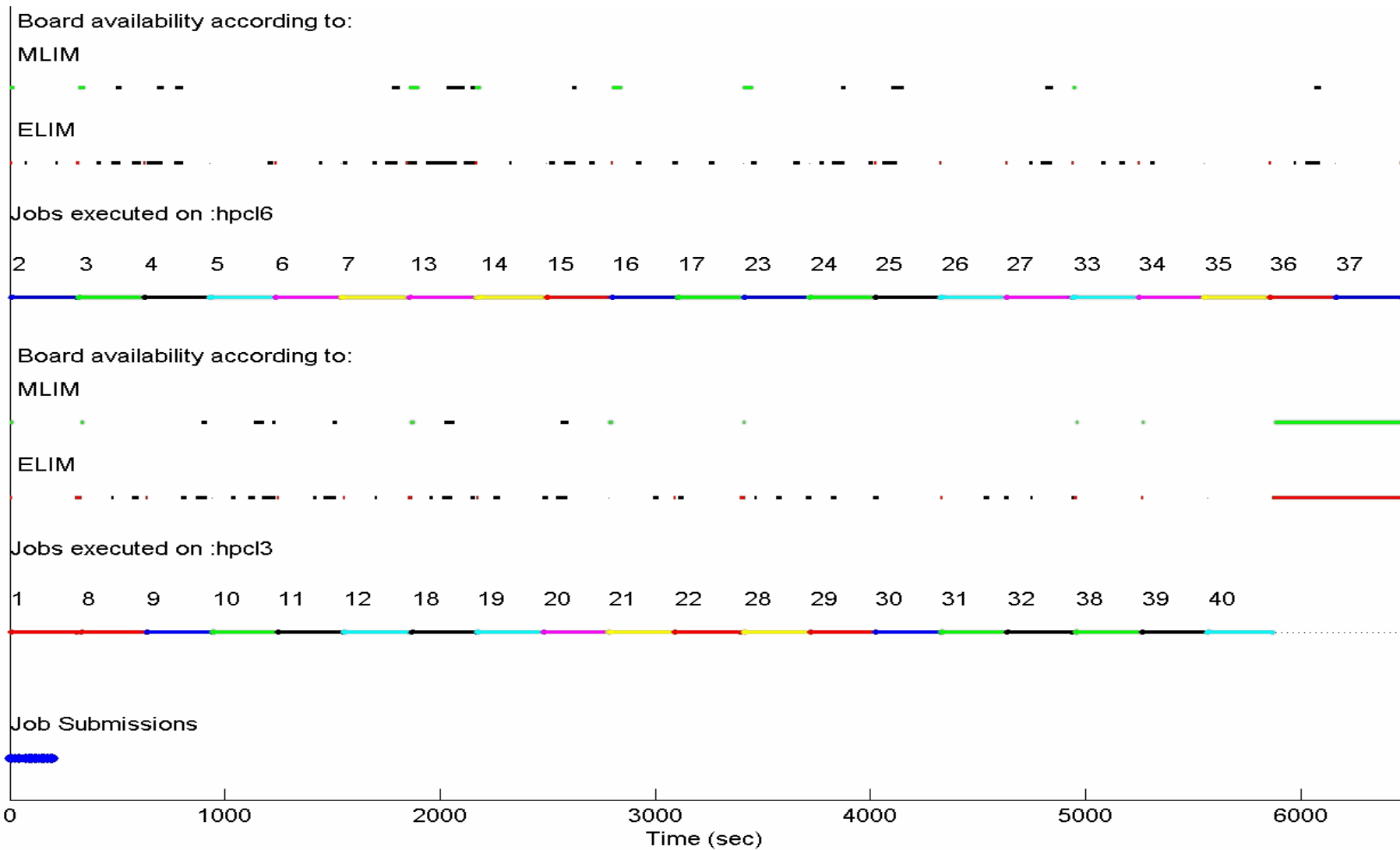
Utilization of machines in Experiment 2, Iteration 1



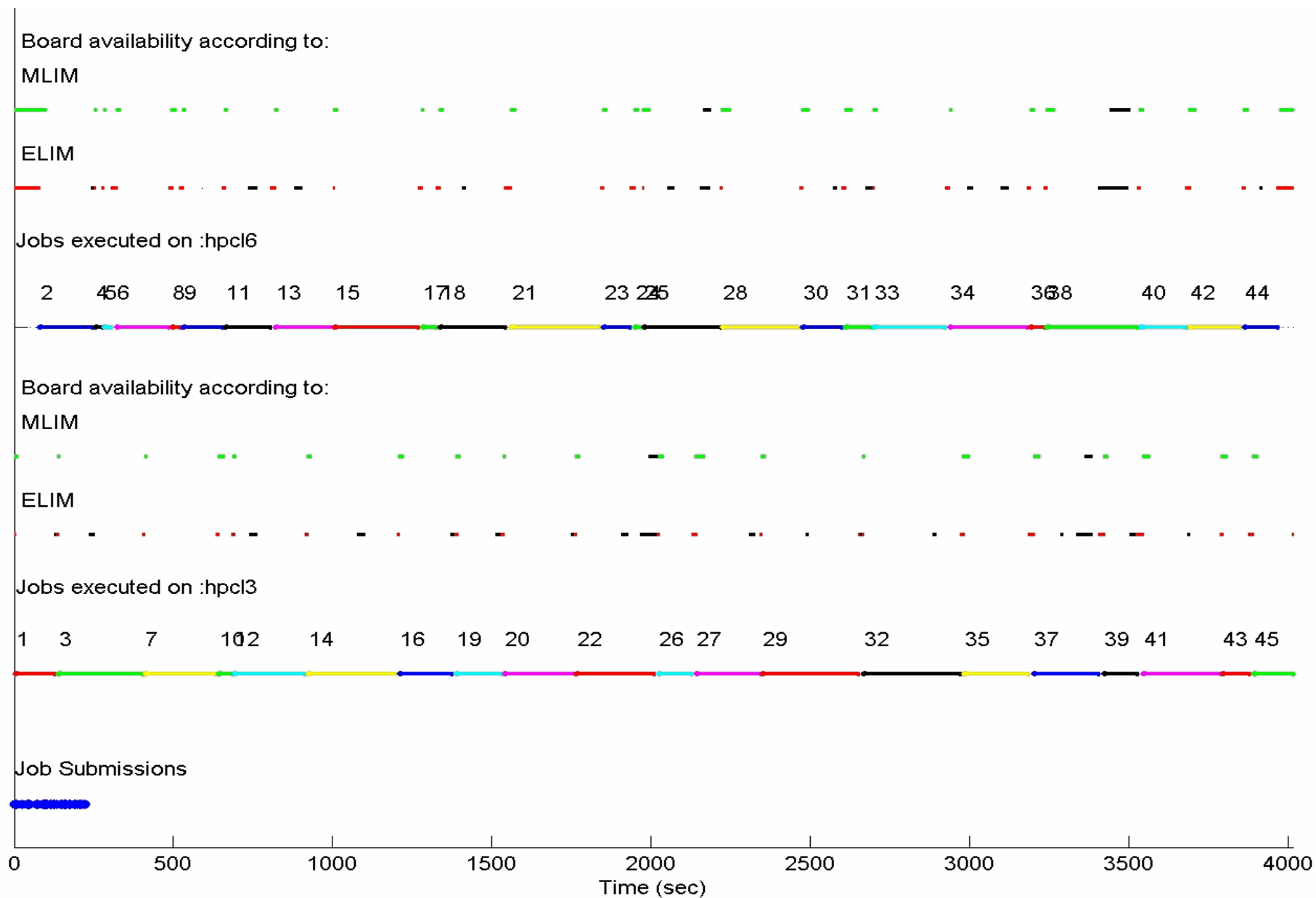
Utilization of machines in Experiment 3, Iteration 1



Utilization of machines in Experiment 4, Iteration 1



Utilization of machines in Experiment 5, Iteration 1



Result

Experiment No.	Utilization [%]		
	iteration 1	iteration 2	iteration 3
1	65.9	78.7	62.8
2	75.6	86.4	84.4
3	90.8	91.6	92.3
4	95	93.6	94
5	91.9	96.2	93.9

Conclusion

- **An extension of LSF, supporting SLAAC-1V FPGA accelerator boards was developed and experimentally tested**
- **Full implementation and verification of the middleware for SLAAC-1V boards**
- **The architecture was verified experimentally**
- **The utilization of the idle boards was demonstrated to reach up to 95% in our experimental setting which include Linux and Windows NT workstations**